CLAIMS:

1. A differential amplifier circuit for amplifying an input signal and for providing an output signal representative of the input signal, the differential amplifier circuit comprising:

first and second input signal nodes;

a first amplifier circuit operatively connected to the first input signal node;

a second amplifier circuit operatively connected to the second input signal node;

a first coupling circuit including a capacitor and an active element, the first coupling circuit being connected between the first input signal node and the second amplifier circuit; and

a second coupling circuit including a capacitor and an active element, the second coupling circuit being connected between the second input signal node and the first amplifier circuit.

2. The differential amplifier circuit of claim 1 wherein the first and second amplifier circuits each include:

an input transistor having a base, a collector, and an emitter;

a collector circuit connected between a fixed potential and the collector of the input transistor; and

a current generator for directing current through the input transistor and the collector circuit.

3. The differential amplifier circuit of claim 2 wherein the collector circuit of each of the amplifier circuits includes a cascode stage.

4. The differential amplifier circuit of claim 3 wherein the cascode stage of each of the amplifier circuits comprises:

a cascode transistor having a base, a collector, and an emitter, wherein the base is connected to a bias potential, and the emitter is connected to the collector of the input transistor of the respective amplifier circuit; and

a resistor connected between the fixed potential and the collector of the cascode transistor.

5. The differential amplifier circuit of claim 1 wherein the first and second coupling circuits each comprises:

a transistor having a base, a collector, and an emitter, wherein the base is connected to the corresponding input signal node, and the collector is connected to a fixed potential;

a capacitor connected between the emitter of the transistor and the base of the input transistor of the corresponding amplifier circuit; and

a current generator for directing current through the transistor.

6. A read system for reading information from a magnetic storage medium using a magnetoresistive head and for providing an output signal representative of the information read, the read system comprising:

first and second input signal nodes for connection to the magnetoresistive head;

a first amplifier circuit operatively connected to the first input signal node;

a second amplifier circuit operatively connected to the second input signal node;

a first coupling circuit including a capacitor and an active element, the first coupling circuit being connected between the first input signal node and the second amplifier circuit; and

a second coupling circuit including a capacitor and an active element, the second coupling circuit being connected between the second input signal node and the first amplifier circuit.

7. The read system of claim 6 wherein the first and second amplifier circuits each include:

an input transistor having a base, a collector, and an emitter;

a collector circuit connected between a fixed potential and the collector of the input transistor; and

a current generator for directing current through the input transistor and the collector circuit.

8. The read system of claim 7 wherein the collector circuit of each of the amplifier circuits includes a cascode stage.

9. The read system of claim 8 wherein the cascode stage of each of the amplifier circuits comprises:

a cascode transistor having a base, a collector, and an emitter, wherein the base is connected to a bias potential, and the emitter is connected to the collector of the input transistor of the respective amplifier circuit; and

a resistor connected between the fixed potential and the collector of the cascode transistor.

10. The read system of claim 6 wherein the first and second coupling circuits each comprises:

a transistor having a base, a collector, and an emitter, wherein the base is connected to the corresponding input signal node, and the collector is connected to a fixed potential;

a capacitor connected between the emitter of the transistor and the base of the input transistor of the corresponding amplifier circuit; and

a current generator for directing current through the transistor.

11. In a read system that includes first and second input signal nodes for connection to a magnetoresistive head, that includes first and second input transistors, and that includes first and second collector circuits connected between a fixed potential and the respective first and second input transistors, the improvement comprising:

a first coupling circuit comprising a first coupling transistor having a base connected to the first input signal node, a collector connected to the fixed potential, and an emitter ac coupled to the second input transistor, and a current generator for directing current through the first coupling transistor; and

a second coupling circuit comprising a second coupling transistor having a base connected to the second input signal node, a collector connected to the fixed potential, and an emitter ac coupled to the first input transistor, and a current generator for directing current through the second coupling transistor.

12. The read system of claim 11 wherein a first capacitor is connected between the emitter of the first coupling transistor and the second input transistor,

and a second capacitor is connected between the emitter of the second coupling transistor and the first input transistor.

13. A read system for reading information from a magnetic storage medium using a magnetoresistive head and for providing an output signal representative of the information read, the read system comprising:

first and second input signal nodes for connection to the magnetoresistive head;

a first transistor having a base, a collector, and an emitter, wherein the emitter is connected to the first input signal node;

a second transistor having a base, a collector, and an emitter, wherein the emitter is connected to the second input signal node;

a third transistor having a base, a collector, and an emitter, wherein the emitter is connected the collector of the first transistor, and the base is connected to a bias potential;

a fourth transistor having a base, a collector, and an emitter, wherein the emitter is connected the collector of the second transistor, and the base is connected to the bias potential;

a first resistor connected between the collector of the third transistor and a first fixed potential;

a second resistor connected between the collector of the fourth transistor and the first fixed potential;

a first current generator connected between the emitter of the first transistor and a second fixed potential;

a second current generator connected between the emitter of the second transistor and the second fixed potential;

a fifth transistor having a base, a collector, and an emitter, wherein the base is connected to the second input signal node, and the collector is connected to the first fixed potential;

a sixth transistor having a base, a collector, and an emitter, wherein the base is connected to the first input signal node, and the collector is connected to the first fixed potential;

a first capacitor connected between the emitter of the fifth transistor and the base of the first transistor;

a second capacitor connected between the emitter of the sixth transistor and the base of the second transistor;

a third current generator connected between the emitter of the fifth transistor and the second fixed potential; and

a fourth current generator connected between the emitter of the sixth transistor and the second fixed potential.

14. A method of amplifying an input signal from a magnetoresistive head, the input signal comprising a differential signal including a first signal provided at a first input signal node and a second signal provided at a second input signal node, the first and second input signal nodes being connected to opposite sides of the magnetoresistive head, the method comprising:

amplifying the first signal with a first amplifier circuit to provide an amplified first signal;

amplifying the second signal with a second amplifier circuit to provide an amplified second signal;

coupling a first capacitor and a first active element between the first input signal node and the second amplifier circuit; and

coupling a second capacitor and a second active element between the second input signal node and the first amplifier circuit.

15. The method of claim 14, wherein the step of amplifying the first signal with the first amplifier circuit comprises:

coupling a first amplifier transistor to the first input signal node;

coupling a first cascode transistor to the first amplifier transistor; and

coupling a first resistor to the first cascode transistor, the amplified first signal being provided between the first resistor and the first cascode transistor.

16. The method of claim 15, wherein the step of amplifying the second signal with the second amplifier circuit comprises:

coupling a second amplifier transistor to the second input signal node;

coupling a second cascode transistor to the second amplifier transistor; and

coupling a second resistor to the second cascode transistor, the amplified second signal being provided between the second resistor and the second cascode transistor.

17. The method of claim 16, wherein the step of coupling the first capacitor and the first active element between the first input signal node and the second amplifier circuit comprises:

connecting the first capacitor between the first input signal node and the second amplifier transistor; and

connecting the first active element in parallel with the first capacitor between the first input signal node and the second amplifier transistor.

18. The method of claim 17, wherein the step of coupling the second capacitor and the second active element between the second input signal node and the first amplifier circuit comprises:

connecting the second capacitor between the second input signal node and the first amplifier transistor; and

connecting the second active element in parallel with the second capacitor between the second input signal node and the first amplifier transistor.

19. The method of claim 18, wherein the step of connecting the second active element in parallel with the second capacitor between the second input signal node and the first amplifier transistor comprises:

connecting a control element of the second active element to the second input signal node; and

connecting a controlled element of the second active element to a control element of the first amplifier transistor.

20. The method of claim 17, wherein the step of connecting the first active element in parallel with the first capacitor between the first input signal node and the second amplifier transistor comprises:

connecting a control element of the first active element to the first input signal node; and

connecting a controlled element of the first active element to a control element of the second amplifier transistor.